

CT saturation and its influence on protective relays

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RESUMEN

En este artículo se revisa el fenómeno de saturación CT y los factores que la afectan. Describe su influencia sobre las diferentes funciones de protección, tales como la sobre corriente, direccional, diferencial, y distancia, y explica las soluciones aplicadas por relé de última generación para incrementar la seguridad y dependabilidad durante la saturación CT. También muestra como dimensionar un CT basándose en los estándares de hoy en día.

PALABRAS CLAVE

CT saturación, CT dimensionamiento, dc offset, remanente, sobre corriente, direccional, diferencial, distancia.

ABSTRACT

This paper reviews the phenomena of Current Transformer saturation and the factors that affect it. It describes the influence CT saturation has on the different protection functions such as overcurrent, directional, differential and distance and explains the solutions applied by last generation relays to increase the security and dependability during CT saturation. The paper also shows how to dimension a CT based on the different standards used nowadays.

KEYWORDS

CT saturation, CT dimensioning, dc offset, remanence, overcurrent, directional, differential, distance.

INTRODUCTION

CT saturation occurs when the CT flux reaches the knee point of the magnetizing curve. It is affected by several factors such as fault current magnitude, CT burden, fault current dc offset, remanent flux, etc. CT saturation generates “gaps” in the current waveform, affecting any current-based protection function, either using instantaneous values or phasors, decreasing the current magnitude and leading its phase. CT saturation will affect the following protection functions:

Overcurrent: Phase overcurrent units will tend to increase the tripping times as the phase current is underestimated. On the other hand, the directional units that supervise the overcurrent units will be affected by the angle error.

Differential: CT saturation will create a false differential current during external faults affecting the protection stability. In the transformer differential protection the harmonic blocking may operate for internal faults with CT saturation, delaying the trip of the percentage differential protection.

The current magnitude reduction and the phase leading, both combined, may cause underreach or overreach of the distance units, depending on the shape of the distance characteristics.

This paper explains the phenomena of CT saturation and the different factors that affect it. It also describes the solutions applied by last generation relays to cope with CT saturation, like saturation detectors, external fault detectors, directional comparison units, measurement algorithms based on peak values or on shorter windows, etc. It also explains how these solutions reduce the CT sizing requirements.

CT FUNDAMENTALS
CT equivalent circuit

Figure 1 shows the equivalent circuit of a CT. Current i'_1 represents the primary current referred to the secondary winding:

$$i'_1 = i_1 \frac{N_2}{N_1}, \tag{1}$$

where N_1 and N_2 are the number of primary and secondary turns, respectively. As current i'_1 is defined by the primary power system, i'_1 is represented by a current source, therefore the primary leakage impedance can be removed as it does not have any effect in the CT circuit. On the other hand, the reactive components in the circuit may be neglected, considering a pure resistive burden ($X_s \approx 0$ and $Z_{burden} = R_b$). The burden impedance is equal to the sum of the wire impedance, mostly resistive, and the relay impedance, negligible for digital relays. The circuit of figure 1 is, therefore, simplified to the circuit of figure 2.

The power supplied by the CT is:

$$P = v_b i_2 = i_2^2 R_b. \tag{2}$$

The magnetizing voltage will be:

$$e_m = i_2 (R_{ct} + R_b). \tag{3}$$

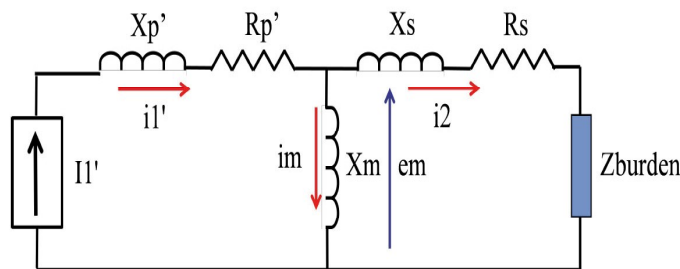


Fig. 1. Equivalent circuit of a CT.

CT saturation

By applying the Lenz law, the magnetizing voltage e_m is:

$$e_m = i_2 (R_{ct} + R_b) = N_2 \frac{d\phi}{dt}, \tag{4}$$

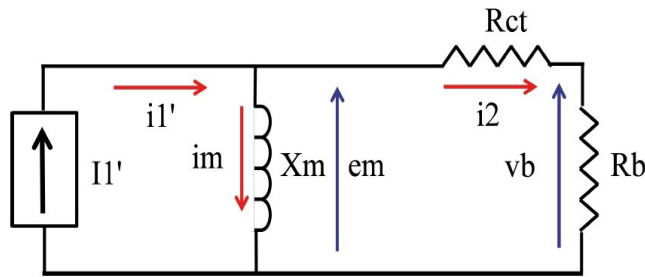


Fig. 2. Simplified equivalent circuit of a CT

therefore

$$\phi = \frac{1}{N_2} \int_0^t i_2 (R_{ct} + R_b) dt. \quad (5)$$

The X_m reactance is non-linear and the CT flux and the magnetizing current, i_m , follows the typical characteristic represented in figure 3.

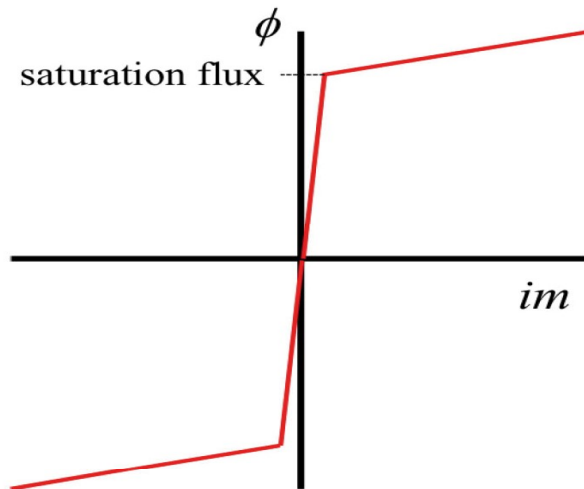


Fig. 3. CT magnetizing curve.

During normal conditions the flux value will be lower than the saturation flux, therefore the magnetizing current, i_m , will be very low (X_m will be very high) and so i_2 will practically equal i_1' . However, if the flux increases because of a high secondary current i_2 and/or a high $R_{ct} + R_b$ impedance, and it reaches the saturation flux, the magnetizing current will increase very much (X_m will be very low), making i_2 to have very reduced values. As the flux is sinusoidal, it will have values above and below the saturation flux, making the CT entering and leaving saturation. During the saturation periods, current i_2 will be practically zero and current i_m will equal i_1' . Figure 4 shows the secondary current, the magnetizing current and the flux in a CT. The red curves correspond to a saturated CT and the blue curves to a non-saturated CT (ideal CT with linear magnetizing characteristic). Note that during the CT saturation periods the flux is practically constant, the secondary current practically zero and the magnetizing current is practically equal to the secondary current of the ideal CT. Figure 5 shows the magnetizing curve of the real CT.

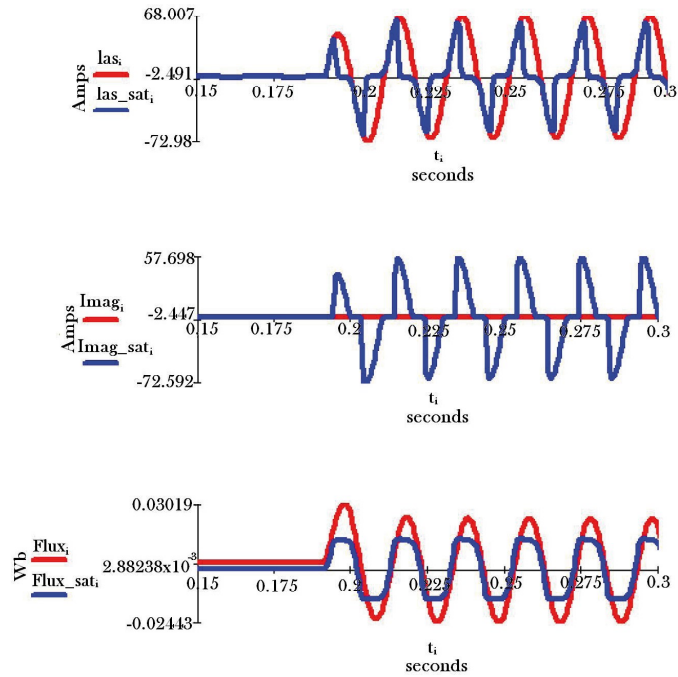


Fig. 4. Secondary current, magnetizing current and flux in a saturated and non-saturated CT (no dc offset included).

Influence of dc offset

There is another factor, apart from the current magnitude and the burden value, that makes the CT flux increase: the dc offset in the current.

In the circuit of figure 6, the following equation is fulfilled:

$$E = Ri + L \frac{di}{dt}. \tag{6}$$

When the switch S is closed, simulating the occurrence of a fault, a transient state occurs during which the current follows

$$i(t) = I \left[e^{-\frac{t}{T_1}} \cos(\gamma - \varphi) - \cos(\omega t + \gamma - \varphi) \right], \tag{7}$$

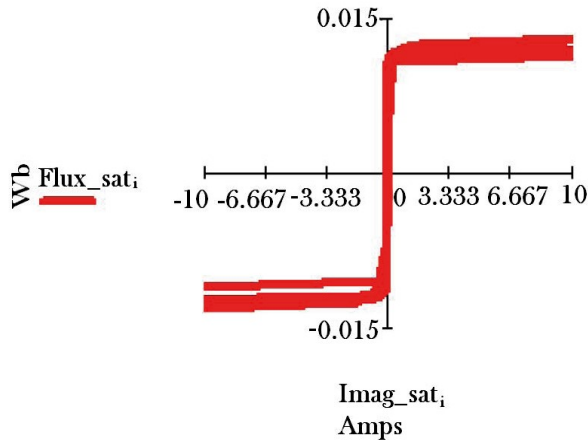


Fig. 5. Flux vs. magnetizing current curve.

where

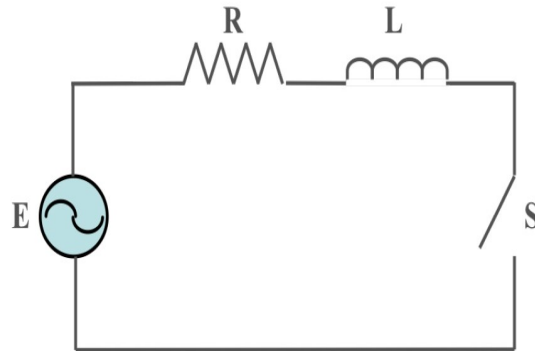


Fig. 6. RL circuit.

$$I = \frac{E}{\sqrt{R^2 + (\omega L)^2}}, \quad (8)$$

$$\varphi = \arctan\left(\frac{\omega L}{R}\right), \quad (9)$$

y

$$T_1 = \frac{L}{R}. \quad (10)$$

Let's analyze the flux waveform when $i'_1(t)=i(t)$. In order to simplify the latter equations we will consider $\theta=\gamma-\varphi$.

Analysis not considering X_m . If we consider $X_m \approx \infty$, $i_2 = i'_1$, therefore

$$\begin{aligned} \phi &= \frac{1}{N_2} \int_0^t i'_1 (R_{ct} + R_b) dt \\ &= \frac{1}{N_2} \int_0^t I \left[e^{-\frac{t}{T_1}} \cos(\gamma - \varphi) - \cos(\omega t + \gamma - \varphi) \right] (R_{ct} + R_b) dt. \end{aligned}$$

Assuming $\phi(0) = 0$

$$\phi(t) = \frac{1}{N_2} I \left[T_1 \left(1 - e^{-\frac{t}{T_1}} \right) \cos\theta - \frac{1}{\omega} \sin(\omega t + \theta) \right] (R_{ct} + R_b) \quad (11)$$

Figure 7 shows, at the top, a current wave with and without dc offset and the flux that corresponds to each current wave at the bottom. As it can be observed when the current includes dc offset the flux grows very much, which can make the CT saturate. As the flux represents the area under the integrated waveform, when the latter one includes a dc offset, the positive and negative areas will be different (in the case shown in figure 7 the positive area is higher than the negative one), therefore they will not cancel each other, making the flux increase continuously.

Figure 8 shows the secondary current, the magnetizing current and the flux in a CT. The red curves correspond to a saturated CT and the blue curves to a non-saturated CT (ideal CT). In the saturated CT, when the flux reaches the saturation flux (see the magnetizing curve in figure 9), its growth is stopped, i_2 current tends to zero and i_m current tends to equal i'_1 current. The flux increase is stopped when it reaches the saturation flux by reducing the positive area below current i_2 , making i_2 practically zero and, therefore, “cutting” the i_2 waveform. When the flux is below the saturation flux, the CT leaves the saturation state, i_2 gets normal values and i_m is practically zero. Saturation and non-saturation periods alternate until the CT definitively gets out of saturation.

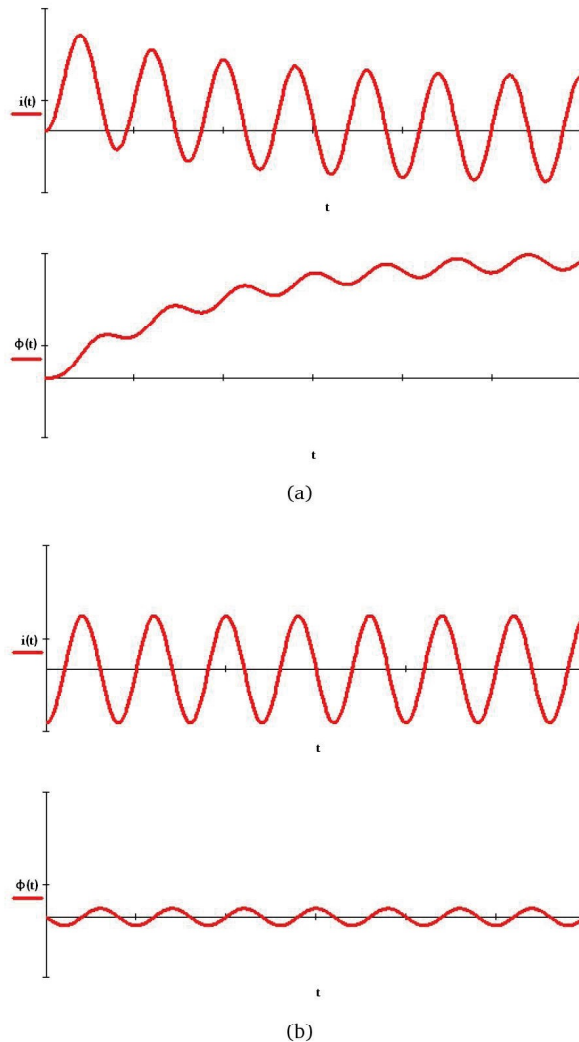


Fig. 7. Current and flux (a) with dc offset and (b) without dc offset.

Analysis considering X_m . If X_m is considered, the flux can be calculated as

$$\begin{aligned} \phi &= \frac{1}{N_2} \int_0^t L_m \frac{di_m}{dt}, \\ &= \frac{1}{N_2} L_m i_m(t). \end{aligned} \tag{12}$$

L_m is calculated as

$$\begin{aligned}
 L_m \frac{di_m}{dt} &= (R_{ct} + R_b) i_2, \\
 &= (R_{ct} + R_b) (i'_1 i_m), \\
 L_m \frac{di_m}{dt} + (R_{ct} + R_b) i_m &= (R_{ct} + R_b) i'_1, \\
 \frac{L_m}{(R_{ct} + R_b)} \frac{di_m}{dt} + i_m &= i'_1.
 \end{aligned} \tag{13}$$

Calling

$$T_2 = (R_{ct} + R_b), \tag{14}$$

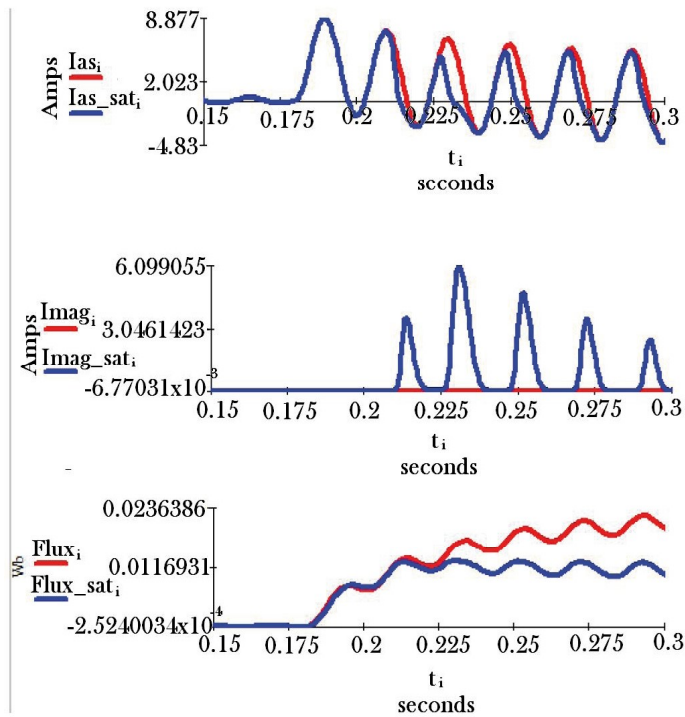


Fig. 8. Secondary current, magnetizing current and flux in a saturated and non-saturated CT (dc offset included).

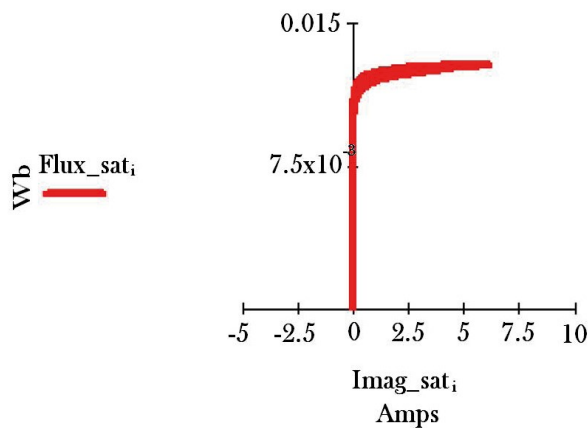


Fig. 9. Flux vs. Magnetizing current curve.

we can get.¹

$$\begin{aligned} \phi = \frac{1}{N_2} I \left[\frac{T_1}{T_1 - T_2} \cos \theta \left(e^{-\frac{t}{T_1}} - e^{-\frac{t}{T_2}} \right) + \right. \\ \left. + \frac{1}{\omega^2 + T_2^2 + 1} \left[(\omega T_2 \sin \theta + \cos \theta) e^{-\frac{t}{T_1}} + \right. \right. \\ \left. \left. - (\omega T_2 \sin(\omega t + \theta) + \cos(\omega t + \theta)) \right] \right] L_m. \end{aligned} \quad (15)$$

Influence of flux remanence

When the primary current in a CT is interrupted, a remanent flux will remain in the magnetic circuit. Its magnitude will depend on the flux in the CT core at the time of current interruption.

If this flux was very high due to a high dc offset and/or a high symmetrical current and/or a high burden, the remanent flux will be high.

Once the remanent flux has been established, very little is dissipated under normal conditions, therefore it will remain in the core until it is demagnetized. In non-gapped CTs the remanent flux may be up to 80% of the saturation flux.

The remanent flux will affect the transient behavior of the CT. It will add or subtract the flux created by the current magnitude, burden value and dc offset. Depending on the sign of the remanent flux compared with the sign of the flux created by the other mechanisms, it will worsen or improve the CT transient response.

The remanent flux should be especially considered for reclose onto fault conditions. Figure 10 shows the effect of a permanent fault on the CT wired to a line relay (the first plot represents the current and the second one the flux). It can be observed that the CT saturation is heavier when reclosing onto fault than during the initial fault.

With regard to the remanence, there are three types of CTs:

High remanence CT: no limit for the remanence is specified. The CT has no air-gap. The remanent flux can reach 80% of the saturation flux. Examples of such CTs are: class P, PX, TPX (IEC60044 and IEC61869-2), TPS (IEC60044-6), P or X (BS 3938) and non-gapped class C (IEEE C57.13).

Low remanence CT: a remanence limit is specified. In classes PRLow remanence CT: a remanence limit is specified. In classes PR IEC61869-2) and TPY (IEC60044-6 and IEC61869-2) the specified remanence factor (remanent flux/saturation flux) must be lower than 10%. This type of CTs includes small air-gaps.

No remanence CT: the remanent flux is practically negligible. Class TPZ (IEC60044-6 and IEC61869-2) is a non-remanence CT. This type of CT includes bigger air-gaps.

CT dimensioning

Class P of IEC 61869-2 standard

The CT is specified with the following data:

- Rated transformation ratio: the ratio of the rated primary current to the rated

secondary current, e. g. 600/5.

- Rated power: power provided by the CT at rated current and rated burden, e.g. 10 VA.
- Accuracy class: 5P and 10P defines a maximum composite error of 5% or 10% at the accuracy limit current (accuracy limit factor (ALF) multiplied by the rated current).
- Accuracy limit factor: times the rated current, without dc offset, at which the accuracy class is fulfilled.
- Secondary internal resistance: R_{ct} in figure 2.

The CT will be adequate if $K_{total} = K_{ssc} K_b K_{rf} K_{rem} < ALF$, where K_{ssc} is the symmetrical short-circuit current factor, K_b is the burden factor, K_{rf} is the overdimensioning factor for dc offset, and K_{rem} is the remanence overdimensioning factor.

Symmetrical short-circuit current factor K_{ssc} . It is the ratio between the maximum short circuit current and the rated current.

Burden factor K_b . It is the ratio

$$\frac{R_s + R_{burden}}{R_s + R_n},$$

where R_n is the rated burden. R_n can be calculated from the CT rated power:

$$R_n = \frac{P_n}{I_{2n}^2}. \tag{16}$$

The accuracy limit factor is defined for the rated burden. For a different burden the maximum symmetrical current that assures the fulfillment of the accuracy class will be different than the accuracy limit current (it will be higher than the accuracy limit current if the burden is lower than the rated one and it will be lower if the burden is higher than the rated one). This condition is taken into account by the burden factor.

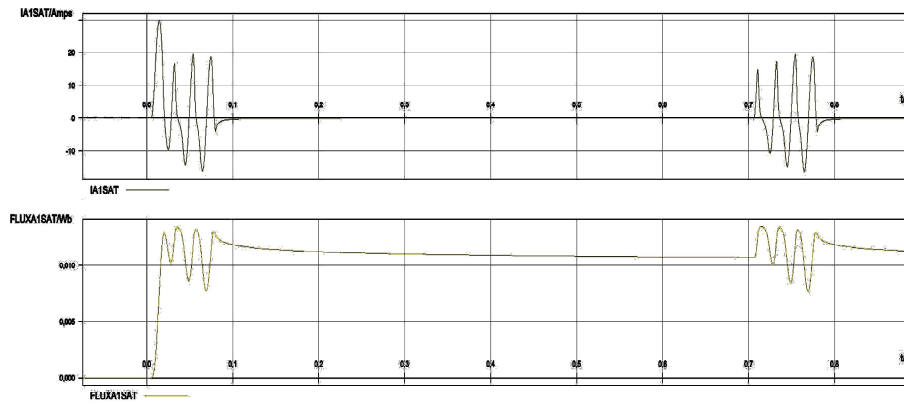


Fig. 10. Current and flux during a trip-reclose-trip cycle.

Transient overdimensioning factor K_{ϕ} . It was seen in *Influence of dc offset* that the flux created by a current with dc offset (asymmetrical current) was much higher than the flux generated by a current without any dc component (symmetrical current). As the ALF factor is defined for a symmetrical current, an overdimensioning factor for asymmetrical currents must be considered. This factor will be given by

$$\frac{\phi_{\max \text{ ac+dc}}}{\phi_{\max \text{ ac}}},$$

which represents the ratio between the maximum total flux (sum of dc and ac fluxes) and the maximum ac flux.

Considering (11), the maximum flux when there is no dc offset in the current is

$$\phi_{\max \text{ ac}} = \frac{1}{N_2} I \frac{1}{\omega} (R_{ct} + R_b). \quad (17)$$

The maximum flux when there is dc offset in the current is obtained for (maximum dc offset) and when the exponential has reached its limit ($t \rightarrow \infty$):

$$\phi_{\max \text{ ac+dc}} = \frac{1}{N_2} I \left(\frac{1}{\omega} + T_1 \right) (R_{ct} + R_b), \quad (18)$$

therefore

$$\begin{aligned} \frac{\phi_{\max \text{ ac+dc}}}{\phi_{\max \text{ ac}}} &= 1 + T_1 \omega, \\ &= 1 + \frac{L}{R} \omega = 1 + \frac{X}{R}. \end{aligned} \quad (19)$$

Considering (15),¹

$$\frac{\phi_{\max \text{ ac+dc}}}{\phi_{\max \text{ ac}}} = 1 + \omega T_2 \left(\frac{T_1}{T_2} \right)^{\frac{T_2}{T_2 - T_1}}. \quad (20)$$

In some systems the X/R ratio may be very high (especially in points close to generators: X/R values of 20–30) giving rise to excessive overdimensioning factors that will require too large CTs, not viable, due to cost and space constraints. In this case it is not possible to assure that the CT is not saturated during the whole fault duration but it is assumed that the CT saturates after a timedelay from the fault inception is the value of the flux after the maximum saturation free time. K_{ϕ} can be calculated with (11) or (15).

Considering (11),

$$\frac{\phi_{\max \text{ ac+dc}}}{\phi_{\max \text{ ac}}} = 1 + \omega T_1 \left(1 - e^{-\frac{t}{T_1}} \right). \quad (21)$$

Considering (15),¹

$$\frac{\phi_{\max \text{ ac+dc}}}{\phi_{\max \text{ ac}}} = \frac{\omega T_1 T_2}{T_1 - T_2} \left(e^{-\frac{t}{T_1}} - e^{-\frac{t}{T_2}} \right) + \sin \theta e^{-\frac{t}{T_2}} - \sin(\omega t + \theta). \quad (22)$$

For saturation free times higher than 15 ms, the maximum flux will be obtained with $\theta = 0$, however, for saturation free times lower than 15 ms, the maximum

flux will be obtained for other fault inception angles. Figure 11 shows the K_{tf} curves for three different θ values ($0^\circ - K_{tf0}$ (maximum dc offset), $90^\circ - K_{tf1}$ (no dc offset) and $45^\circ - K_{tf2}$), considering $T_2 = 3$ s and $T_1 = 0.125$ s. It can be checked that approximately from $t = 14$ ms on, K_{tf0} is always higher than K_{tf1} and K_{tf2} . Figure 12 shows a zoom of figure 11 for times lower than 4 ms. In this case the maximum K_{tf} is K_{tf1} with no dc offset. For each saturation free time tolerated by the protective relay the worst inception angle should be determined.

Remanence overdimensioning factor K_{rem} . The remanent flux may worsen the CT transient response if it has the same sign of the flux generated by the current magnitude, burden value and dc offset. This is considered by the remanence overdimensioning factor where K_r is the remanent factor (maximum remanent flux/saturation flux).

$$K_{rem} = \frac{1}{1 - K_r}, \tag{23}$$

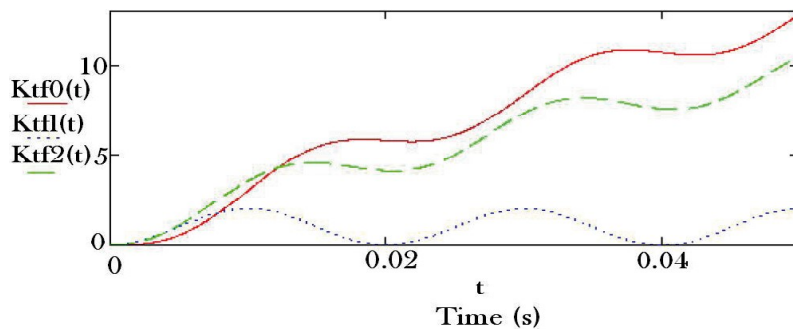


Fig. 11. K_{tf} for different θ values (K_{tf0} , K_{tf1} and K_{tf2} correspond to 0° , 90° and 45° , respectively).

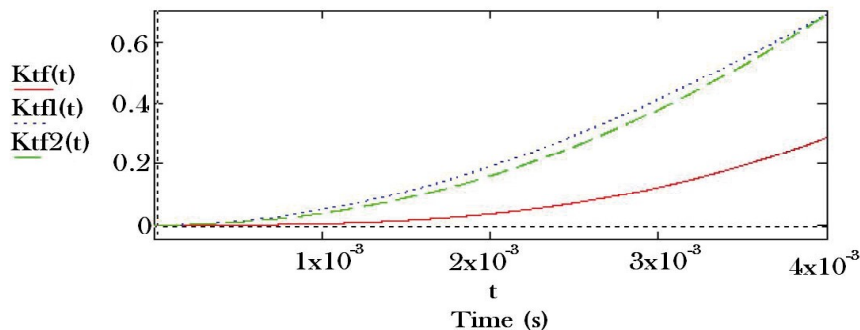


Fig. 12. Zoom of Fig. 11 ($t = 0-4$ ms).

Class C of IEEE C57.13 standard

The most common accuracy class in the IEEE C57.13 standard is the C class. The letter C is followed by a number that indicates the secondary voltage rating, which is defined as the CT secondary voltage that the CT will deliver when it is connected to a standard secondary burden at 20 times the rated secondary current, without exceeding a 10% ratio error. The common standard burdens for protection CTs are 1, 2, 4 and 8 Ω , which correspond, at 5 A rated current, to 100, 200, 400 and 800 V secondary rating voltages (for a C100 CT the voltage

at the 1 Ω burden will be $20 \times 5 \times 1 = 100$ V). With the secondary voltage rating we can obtain the internal magnetizing voltage by adding the voltage drop in the secondary resistance (R_{ct}):

$$E_{m \text{ rated}} = V_b + R_{ct} \times 20I_{2n}. \tag{24}$$

The dimensioning of an IEEE CT can be done by calculating E_m as:

$$E_{m \text{ calc}} = K'_{\text{total}} I_{2n} (R_{ct} + R_b), \tag{25}$$

where $K'_{\text{total}} = K_{\text{ssc}} K_{\text{tf}} K_{\text{rem}}$.

If $E_{m \text{ calc}} < E_{m \text{ rated}} = V_b + R_{ct} 20I_{2n}$ the CT will be valid.

An easier deduction can be made considering that the ALF factor of a C class CT is always 20 (the 10% ratio error cannot be exceeded for a secondary current 20 times the rated current with the rated burden. If $K_{\text{total}} < \text{ALF}$ the CT will be valid.

Class X of BS3938 standard or Class PX of IEC61869-2

Class X CT is defined with:

- Primary and secondary rated currents
- Transformation ratio
- Rated knee-point voltage
- Magnetizing current at rated knee-point voltage
- Resistance of secondary winding

The rated knee-point voltage is defined as the minimum voltage, at rated frequency, applied to the CT secondary terminals which increased by a 10% causes an increase in the magnetizing current of 50% (see figure 13).

The relationship between the rated knee-point voltage (V_{knee}) and the magnetizing voltage at the accuracy limit current with rated burden ($E_{m \text{ rated}}$) is done by approximation, because the definition of the two voltages has no direct relation (V_{knee} has to do with the slope of the magnetizing characteristic and $E_{m \text{ rated}}$ with the current composite error). It is normally considered that $E_{m \text{ rated}} = 1.25$ to 1.3 times V_{knee} .

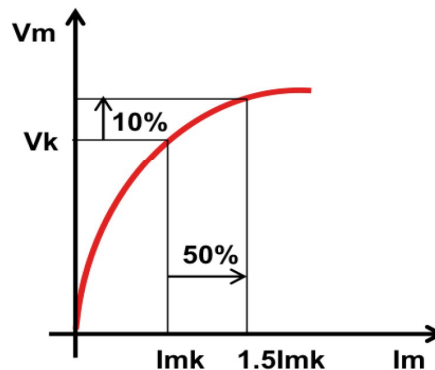


Fig. 13. Knee point voltage definition.

Once $E_{m \text{ rated}}$ is calculated it can be compared with $E_{m \text{ calc}} = K'_{\text{total}} I_{2n} (R_{ct} + R_b)$. The CT will be valid if $E_{m \text{ calc}} < E_{m \text{ rated}}$.

INFLUENCE OF CT SATURATION ON PROTECTIVE RELAYS

Overcurrent

CT saturation introduces errors in the phasor estimation, decreasing the phasor magnitude and leading its phase.² This makes the overcurrent units underestimate the current magnitude giving rise to delayed trips or no trips.

Figure 14 shows the magnitude of the fundamental component of the saturated and non-saturated currents ($|I_A|$ and $|I_{A \text{ sat}}|$, respectively) shown in figure 4. A full-cycle DFT was used for the calculation. It can be seen that the value of the saturated current is much lower than the value of the non-saturated one. Figure 14 also shows the true rms value ($|I_{A \text{ sat rms}}|$); although it is higher than the magnitude of the fundamental frequency of the saturated current, it is still much lower than the magnitude of the fundamental component of the non-saturated current.

For instantaneous units, if the time to saturation is lower than the time it takes for the overcurrent unit to pick-up the trip will be delayed. If the CT saturation is caused by an asymmetrical current, the delay will be approximately equal to the primary time constant, which defines the damping time of the dc offset. If

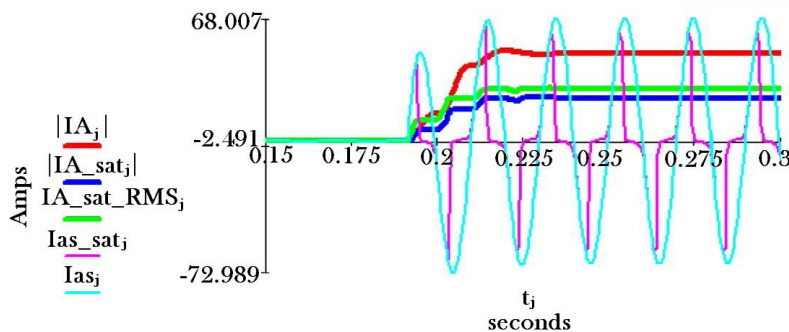


Fig. 14. Magnitude of the fundamental components and true rms value of the saturated and non-saturated currents of figure 4.

the CT saturation was due to a symmetrical current there will not be any trip. In order to increase the dependability of the instantaneous overcurrent units an operation based on the peak value can be used when CT saturation is detected. The implemented algorithm uses the saturation detector described in.³ This detector is based on the derivative of the measured current. At the time that CT saturation initiates there is a significant increase in the derivative. Given that the maximum value of the derivative of the current is

$$A \frac{2\pi}{N},$$

where A is the maximum current and N the number of samples per cycle, when

$$I'_i > kA \frac{2\pi}{N},$$

where k is a constant, the saturation is detected. A is calculated as the greater of two consecutive maxima. The saturation detector will only operate when A exceeds a threshold. The detector includes a reset time of a cycle.

The algorithm based on peak values calculates the dc offset with the difference between two consecutive peak values divided by two. The dc offset is removed to reduce the transient overreach. The overcurrent units based on this algorithm are only enabled when the saturation detector activates and two consecutive peak values have been measured since the activation of a fault detector; figure 15 shows the peak value measured once the dc offset is removed ($I_{\text{peak no dc}}$). Although it is lower than the magnitude of the fundamental component of the non-saturated waveform calculated with a DFT it is much higher than the magnitude of the fundamental component or the true rms value calculated for the saturated waveform.

The algorithm based on peak values requires a saturation free time lower than the algorithm based on full-cycle DFT. For a symmetrical CT saturation it just requires around a quarter of cycle saturation free time for faults in the limit of the reach. For an asymmetrical CT saturation it may require around half-cycle saturation free time. For symmetrical and asymmetrical CT saturation the full-cycle DFT will require one-cycle saturation free-time or higher times if it includes a dc offset filter.

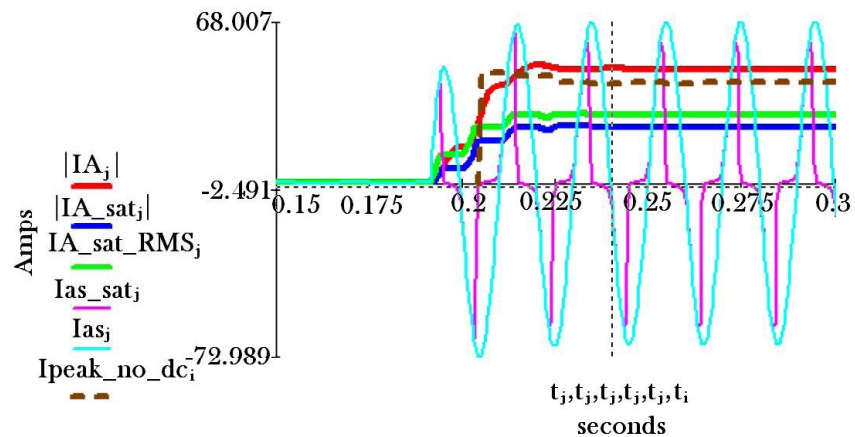


Fig. 15. Magnitude of the fundamental components, true rms value and peak value of the saturated and non-saturated current of figure 4.

For close-in faults the saturation free time for both algorithms, the one based on DFT and the one based on peak values will be much lower than for faults in the limit of the reach. The magnitude obtained with the DFT for the saturated current of figure 14 is around 50% of the magnitude of the non-saturated current. The peak value obtained with the described algorithm is around 90% of the magnitude of the non-saturated current. These values are normally high enough to be above the overcurrent unit pick-up value in the case of a close-in fault. CT remanence should be considered if reclosing is used. The effect of CT saturation on time-delayed overcurrent units is of less importance as the tripping times are normally much higher than the time the CT is in the saturation condition. Anyway, for high primary time constants additional coordination time may be included in

the settings to assure the selectivity. The algorithm based on peak values could also be applied to time-delayed overcurrent units.

Directional unit

Phase directional units normally have a high margin to distinguish the forward faults from the reverse ones. This margin is in the order of 90° . CT saturation makes the phasor angle increase; however it does not normally create an error higher than 90° . To increase the reliability a saturation detector as the one described in *Overcurrent* could be used in order to modify the directional characteristic by slightly reducing the characteristic angle (α in figure 16).

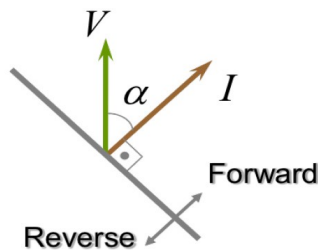


Fig. 16. Directional unit.

Special care should be taken in double breaker bays. In the circuit of Figure 17, if $|I_{sum}|$ is much smaller than $|I_1|$ and $|I_2|$, the errors of the CTs can produce an inversion of the summed current. In this case any directional unit based on this summed current will operate erroneously. In the former situation directional units that compare the currents $|I_1|$ and $|I_2|$ can be implemented. These units may be based on phase currents or sequence currents. Reference⁴ describes the mentioned units.

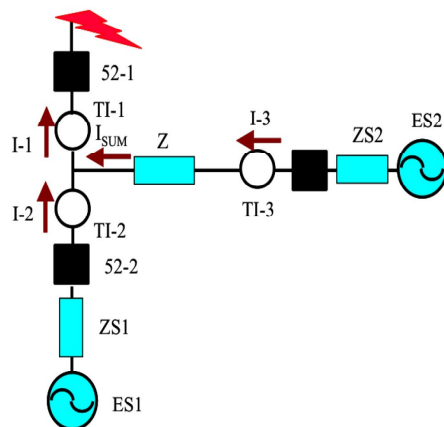


Fig. 17. Reverse fault in a double breaker bay.

Figure 18a and figure 18b show the currents measured by a distance relay in the two CTs of a breaker and a half bay for a reverse AG fault. Figure 18c shows the sum current. As it can be checked, the current measured by CT-2 is slightly distorted, which generates a high distortion in the sum current. The enabled

directional unit was comparing the angle between the phase A positive-sequence voltage and phase A current. The evolution of this angle is shown in Figure 19. As it can be checked, during a small time, the angle is lower than $(\alpha + 90^\circ)$, α is the characteristic angle, set to 84° , which makes the relay trip erroneously. The solution to this false trip was the implementation of a directional unit based on the angle between the currents measured in both CTs of the bay as explained in.⁴ The unit was easily implemented by means of the programmable logic.

Differential units

External faults

For external faults, CT saturation increases the differential current and decreases the restraint current, moving the point (I_{DIF}, I_{REST}) into the operation zone. The through fault current restraint of the percentage differential characteristic is normally not enough to cope with severe CT saturation, therefore units that complement the differential characteristic are normally required.³ Some common units are described below.

Differential unit with instantaneous values. This unit is based on the ratio between the differential and restraint currents. It operates when this ratio is below a threshold. When the fault is external, during the time the CT is not saturated, the ratio will be very small. Figure 20 shows, for an external fault, and for the phase A, the currents at both ends of the protected element, 1 and 2, the differential and restraint currents. This external fault makes CT in winding 1 saturate. As it can be observed, since the activation of a fault detector (signal F_{DET} , based

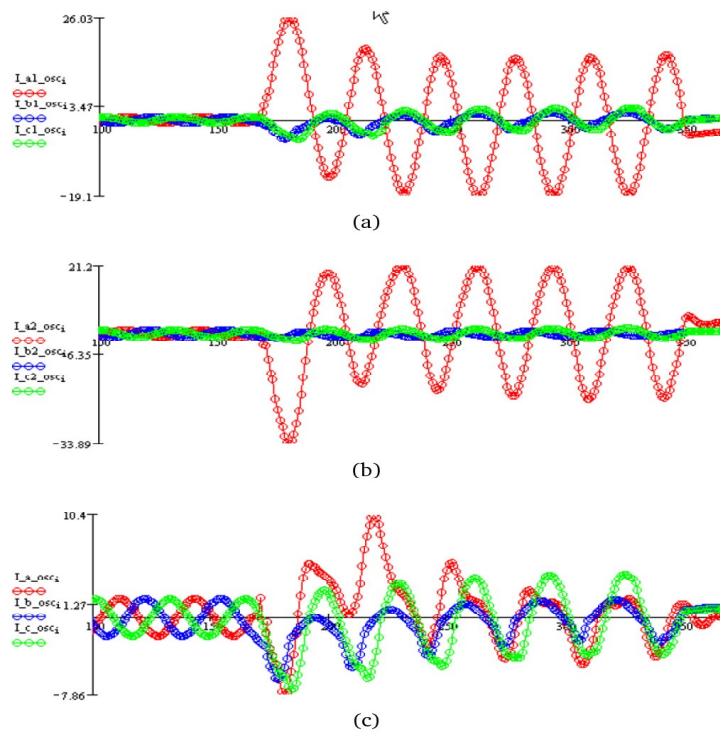


Fig. 18. Currents measured by (a) CT-1 and (b) CT-2, and (c) sum current for a reverse fault in a breaker and a half bay.

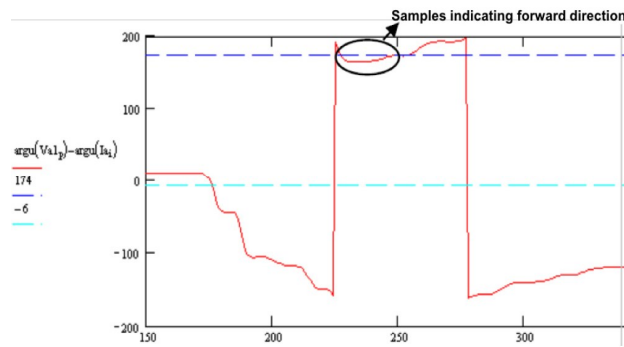


Fig. 19. Angle between V_{a1} and I_a .

on a current change), there will be a consecutive number of samples for which the ratio IDIF /IREST is very low. If this happens, the external fault condition will be activated. More information can be found on.⁵⁻⁷ This unit requires a low saturation free time. Typical times are around 3–4 ms.

Directional comparison units. Ref³ describes a directional comparison unit that uses the angle between the currents measured at each end of the protected element in order to determine if the fault is internal or external. When this angle is lower than 90° the fault is considered internal; on the contrary, if the angle is higher than 90° the fault is considered external (see figure 21). The angular comparison requires that the currents are above a minimum threshold. Two directional comparison units are described, one that operates with phase currents and another one that operates with positive-sequence pure fault current.

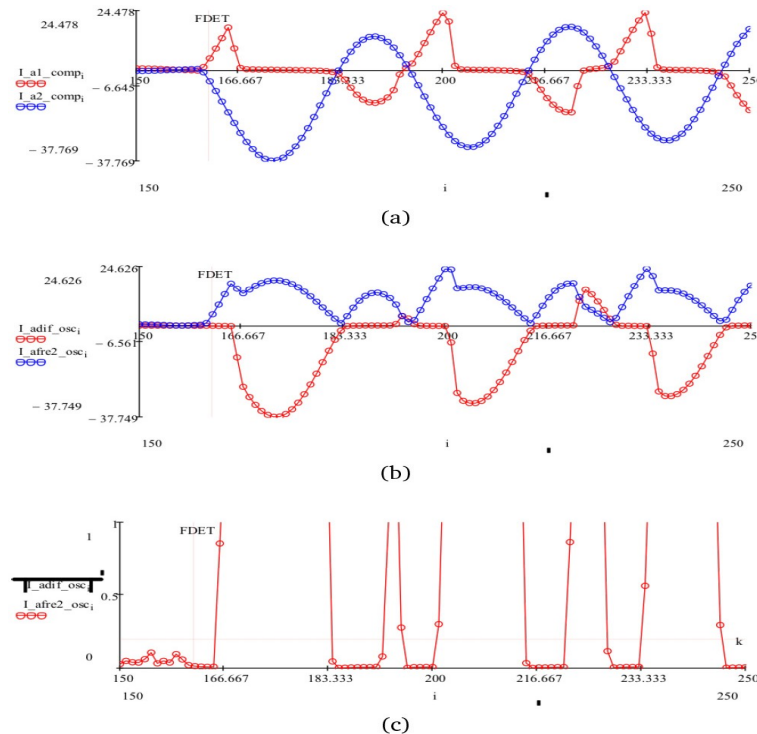


Fig. 20. Currents measured (a) at both ends of the protected element, (b) differential and restrained currents, and (c) ratio between differential and restrained currents for an external fault with CT-1 saturated.

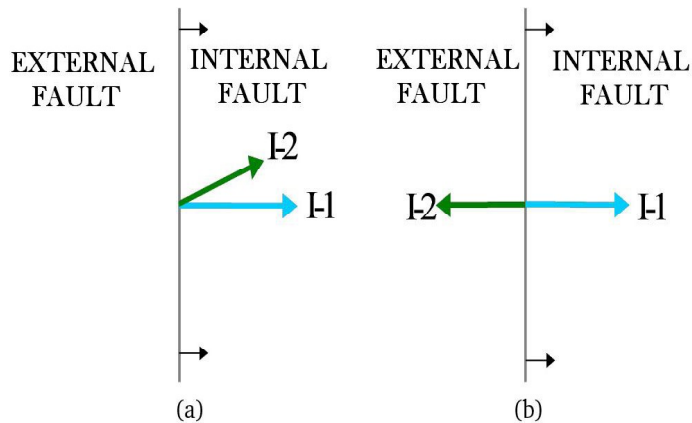


Fig. 21. Directional comparison criteria: (a) internal fault and (b) external fault.

Phase directional comparison unit: the currents must be above the maximum load current. This condition assures that internal weak infeed faults do not generate an external fault indication. To check that the currents are above the load current an algorithm based on the current derivative is used.

The phase directional comparison units may be implemented with instantaneous values instead of phasors, by comparing the sign of the currents at all the ends of the protected element.⁷ If any of the currents has opposite sign as compared with the rest of the currents during several samples an external condition is activated.

Positive-sequence directional comparison unit: it uses pure fault current by removing the prefault current. This makes the unit compensate the load flow effect. The prefault current is taken two cycles before the activation of a fault detector, based on current changes.

More information about the mentioned directional units can be found in.³

Both the directional units based on phasors and the directional unit based on instantaneous values tolerate very low saturation free times (typical values of 2–3 ms). This is because of the high margin the directional comparison units have to distinguish external faults from internal ones.

Internal faults

In transformer differential protections CT saturation for internal faults can make harmonic restraint / blocking operate, because of the harmonic content of the differential current during such faults. This will result in delayed trips. An unrestrained differential unit set above the maximum inrush current is normally used to increase the dependability. However, internal faults with CT saturation could happen for current values lower than the ones for the inrush currents.

Reference⁸ describes a dynamic harmonic restraint/blocking that allows fast tripping during internal faults with CT saturation. The algorithm is based on an external fault detector (for inhibiting the second harmonic restraint / blocking) and underexcitation units (for inhibiting the fifth harmonic restraint/blocking). The second harmonic restraint/blocking is inhibited after a settable time from the

power transformer energization. It is enabled again during a settable time once the external fault detector has activated. The fifth harmonic blocking is inhibited if the ratio V/f is below a threshold.

Inrush currents

Due to the high dc offset and long time constants CT saturation during inrush is very common.⁸ Figure 22 shows a CT saturation registered by a busbar differential relay that tripped during an inrush condition. The first plot represents the currents measured by the three bays that fed the inrush current. The second plot represents the differential and restraint currents calculated by the busbar differential protection. In this case, as the phase bay currents were very low, the phase directional comparison unit was not able to activate the external fault condition. An algorithm to slightly increase the minimum pick-up value of the differential characteristic during transformer energization was included to increase the security for inrush conditions.

Distance protection

As CT saturation decreases the current magnitude and leads the current phase, it will increase the impedance magnitude and reduce its angle. This effect will tend to produce underreach of the distance units. The use of sub-cycle units will reduce the required saturation free time, as these units need lower times to take the trip decision⁹ (saturation free times of half-cycle to $\frac{3}{4}$ cycle depending on the fault location). Anyway, for faults in the limit of zone 1, the fast units will not operate, therefore the saturation free times will be increased to 1 cycle and $\frac{1}{4}$ cycle. That is why the worst case scenario for CT dimensioning will be for a fault at the limit of zone 1. In case of reclose onto fault, the remanence factor should be considered. Taking into account that the close onto fault detector will extend zone 1, the worst case scenario will be for a fault at 100% of the line. As zone 1 will be extended to zone 2 (covering normally 120%) the saturation free times will be slightly lower than 1 cycle–1 and $\frac{1}{4}$ cycle.

CT saturation does not only produce underreach of the distance protection but it can also produce overreach, mainly in quadrilateral characteristics. As the impedance angle is reduced, although its magnitude is increased, the impedance can enter the quadrilateral characteristic through the reactance line, as it can be seen in figure 23.

Figure 24 shows the voltages and currents for an ABG fault at 100% of a line. The CT in phases A and B gets saturated. Figure 25 shows the measured AB impedance trajectory during the time the CT is entering and leaving saturation. The impedance was measured by a sub-cycle filter, based on half-cycle DFT. It also shows the sub-cycle distance characteristic related to zone 1 (reaching 80% of zone 1). The X point represents the AB impedance when the CT is not saturated. The error in the measured impedance when the CT is saturated is clearly seen. In order to avoid any overreach the saturation detector described in³ is implemented. The activation of the saturation detector tilts down the reactance line and reduces the resistive reach.⁹

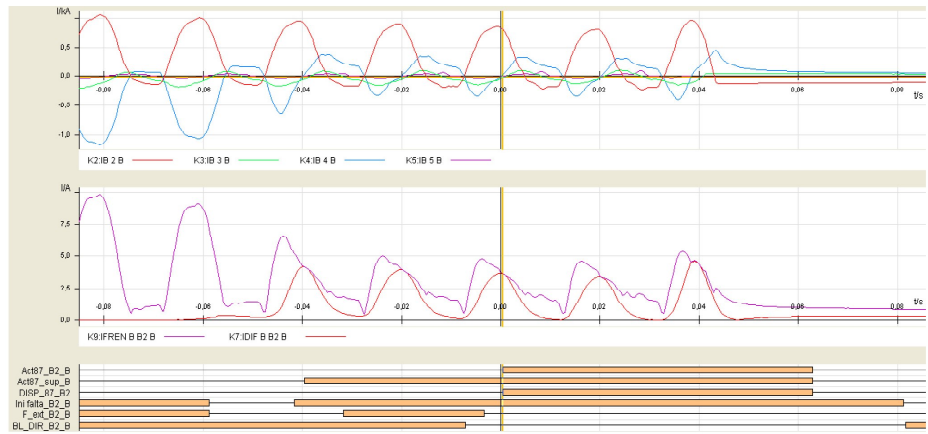


Fig. 22. Phase currents and differential and restraint currents measured by a busbar differential protection during a transformer energization.

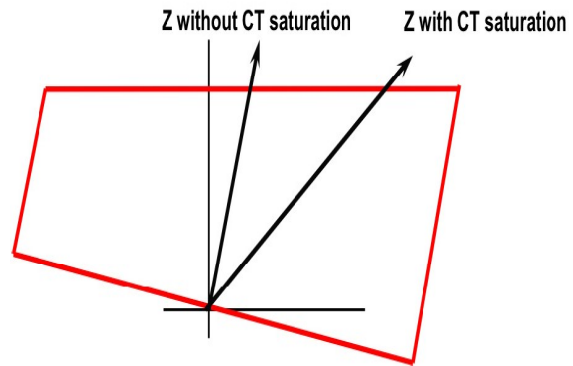


Fig. 23. Measured impedance with and without CT saturation.

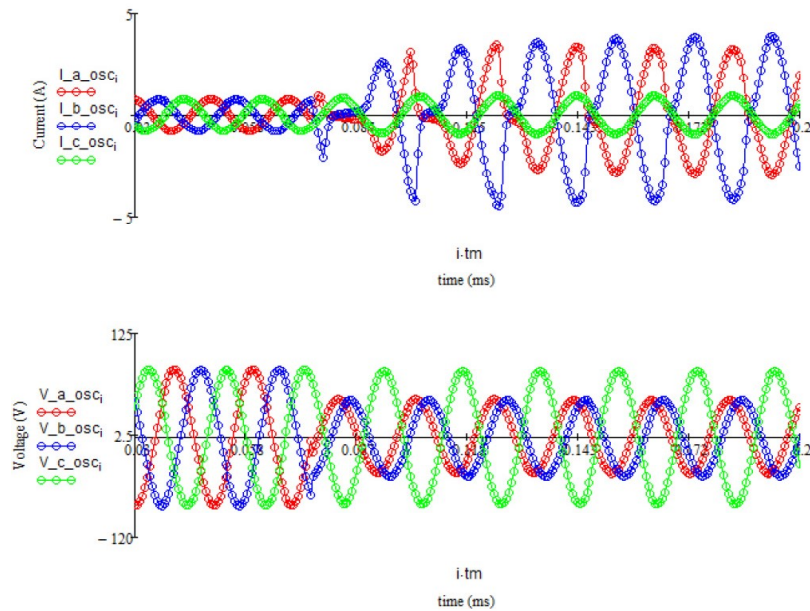


Fig. 24. Voltages and currents for an ABG fault at 100% of the line with CT saturation.

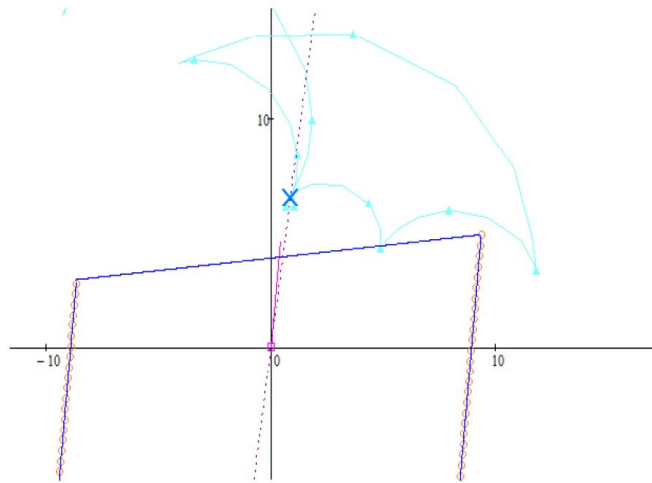


Fig. 25. AB impedance measured with sub-cycle filter for an ABG fault at 100% of the line with CT saturation.

CONCLUSION

CT saturation is affected by the fault current magnitude, the burden value, the dc offset in the fault current and the remanent flux in the CT core. These variables are considered in the following factors: symmetrical short-circuit current factor, burden factor, dc offset overdimensioning factor and remanence overdimensioning factor.

Many times CT saturation cannot be avoided as it will require too large CTs, not viable because of costs and space constraints. In this case protection manufacturers should specify a saturation free time.

New generation relays offer solutions to improve the reliability during CT saturation, relaxing the CT requirements. Some of this solutions are:

- Overcurrent units based on peak values enabled when a CT saturation detector activates.
- Directional units based on dual CT currents to improve the security during reverse faults in breaker and a half bays.
- Complementary units to the differential units such as units that compare the ratio of differential/restraint currents and directional comparison units.
- Dynamic harmonic restraint/blocking: allows disabling the harmonic restraint/blocking during internal faults with CT saturation.
- Sub-cycle distance units complemented with a saturation detector that tilts the reactance line and reduces the resistive reach.

REFERENCES

1. S. Holst and B. S. Palki, “Coordination of fast numerical relays and current transformers — Overdimensioning factors and influencing parameters,” ABB.
2. S. E. Zocholl and D. W. Smaha, “Current transformer concepts,” Proceedings

of the 19th Annual Western Protective Relay Conference, Spokane, Washington, Oct. 1992.

3. R. Cimadevilla, “New protection units included in differential relays,” Proceedings of the 2011 PAC Conference, Dublin, Jun. 2011.
4. R. Cimadevilla, “Protection for Breaker and a Half or Ring Bays,” Proceedings of the 2009 SEAPAC, Melbourne, Mar. 2009.
5. R. Cimadevilla and S. López, “New Requirements for High Voltage Transformer Protection,” Proceedings of the 2009 SEAPAC, Mar. 2009.
6. Instruction Manual, ZIV “Transformer Protection Model IDV”, Zamudio, Spain, Reference BIDV1112Av07.
7. Instruction Manual, ZIV “Busbar Protection Model DBN”, Zamudio, Spain, Reference BDBN0901Av07.
8. R. Cimadevilla, “Inrush currents and their effect on protective relays,” Proceedings of the 2013 TAMU Conference for Protective Relay Engineers, College Station, Texas, Apr. 2013.
9. R. Cimadevilla and I. García, “Sub-cycle distance units: Design, testing and real operation,” Proceedings of the 2015 PAC Conference, Glasgow, June 2015.

